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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/040,055
Filing Date	12/31/2001
First Named Inventor	James K. Falbo
Art Unit	2825
Examiner Name	Yelena Rossoshek
Total Number of Pages in This Submission: 51	**Attorney Docket Number** NTI-030

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Terminal Disclaimer
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Statement Under 37 CFR 3.73(b)
- ☐ CD, Number of CD(s) _____
- ☐ Request for Refund

Remarks

- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

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SIGNATURE OF APPLICANT, ATTORNEY OR AGENT

Firm Name	BEVER, HOFFMAN & HARMS, LLP	Customer Number	29477
Signature			
Printed Name	Jeanette S. Harms		
Date	June 16, 2005	Reg. No.	35,537

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature	Rebecca A Baumann		
Typed or printed name	Rebecca A. Baumann	Date	June 16, 2005

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMV 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818)

FEE TRANSMITTAL For FY 2005

☐ Applicant claims small entity status. See 37 C.F.R. § 1.27

TOTAL AMOUNT OF PAYMENT | **($) 500.00**

Complete if Known	
Application Number	10/040,055
Filing Date	12/31/2001
First Named Inventor	James K. Falbo
Examiner Name	Yelena Rossoshek
Art Unit	2825
Attorney Docket No	NTI-030

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify):_____

☒ Deposit Account Deposit Account Number: **50-0574** Deposit Account Name: **Bever, Hoffman & Harms, LLP**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	**Fees Paid ($)**
Utility	300	150	500	250	200	100	$
Design	200	100	100	50	130	65	$
Plant	200	100	300	150	160	80	$
Reissue	300	150	500	250	600	300	$
Provisional	200	100	0	0	0	100	$

2. EXCESS CLAIM FEES

Fee Description	Fee($)	Small Entity Fee($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee($)	Fee Paid ($)	Multiple Dependent Claims		
	- 20 or HP =	x	=		Fee($)	Fee($)

HP = highest number of total claims paid for, if great than 20

Indep. Claims	Extra Claims	Fee($)	Fee Paid ($)
	- 3 or HP =	x	=

HP = highest number of total claims paid for, if great than 3

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 USC 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee($)	Fee Paid ($)
- 100 =	5- = (round up to a whole number) x		=	

4. OTHER FEE(S)

	Fee Paid ($)
Non-English Specification - $130 fee (no small entity discount)	
Other: **APPEAL BRIEF**	**$500.00**

SUBMITTED BY

Signature:		Registration No. 35,537	Telephone: (408) 451-5907
Name (Print/Type) Jeanette S. Harms			Date: June 16, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James K. Falbo et al.

Assignee: Synopsys Inc.

Title: SHAPE-BASED GEOMETRY ENGINE TO PERFORM SMOOTHING AND OTHER LAYOUT BEAUTIFICATION OPERATIONS

Serial No.: 10/040,055 File Date: December 31, 2001

Examiner: Yelena Rossoshek Art Unit: 2825

Docket No.: NTI-030

June 16, 2005

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

This Appeal Brief, filed in triplicate, is in support of the Notice of Appeal dated June 8, 2005.

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INDEX

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Synopsys, Inc., pursuant to a first Assignment recorded in the U.S. Patent and Trademark Office on December 31, 2001 on Reel 012461, Frame 0224 and a second Assignment recorded in the U.S. Patent and Trademark Office on February 4, 2005 on Reel 015653, Frame 0738.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no other appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 11, 33, 37-43, and 55-99 are pending. Claims 1-10, 12-32, 34-36, and 44-54 are cancelled. Claims 11, 33, 37-43, and 55-99 stand rejected.

In the present paper, rejected Claims 11, 33, 37-43, and 55-99 are appealed.

Pending Claims 11, 33, 37-43, and 55-99 are listed in the Claims Appendix.

IV. STATUS OF AMENDMENTS

No amendments were made to the claims after the Final Office Action dated March 11, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Applicants provide a system and method for efficiently performing layout beautification on an IC layout (or a portion of an IC layout). The concepts of "layout beautification" and "layout imperfections" are critical to understanding the claimed invention. As taught by Applicants in the Specification (emphasis added):

> [0003] Automated design tools can be used to perform various operations on an IC layout. For example, an automated tool might be used to make optical proximity correction (OPC) modifications or perform design rule checking (DRC) on an IC layout. An automated tool could even be used to create the actual IC layout from a design netlist.
>
> [0004] However, while automated tools enable the accurate creation of IC layouts, the complex interactions of the rules embodied in those tools can result in layout imperfections. In other words, while the results of an automated tool may be electrically correct (and even optically correct), the polygons that make up the actual IC layout might include unintended irregularities. These "layout imperfections" are not necessarily defects in the sense that the IC layout may still be electrically correct. However, these layout imperfections may adversely affect layout printability or device performance. Also, such imperfections can significantly increase data volume for a particular IC layout, thereby undesirably increasing layout processing (e.g., OPC, DRC, etc.) and mask production times.

Applicants describe an exemplary layout imperfection (see Fig. 1a) and how a layout imperfection can cause significant problems (see Fig. 1b) compared to a layout without an imperfection (see Fig. 1c). Figs. 1a, 1b, and 1c and the paragraphs in the Specification describing these figures are shown below for convenience.

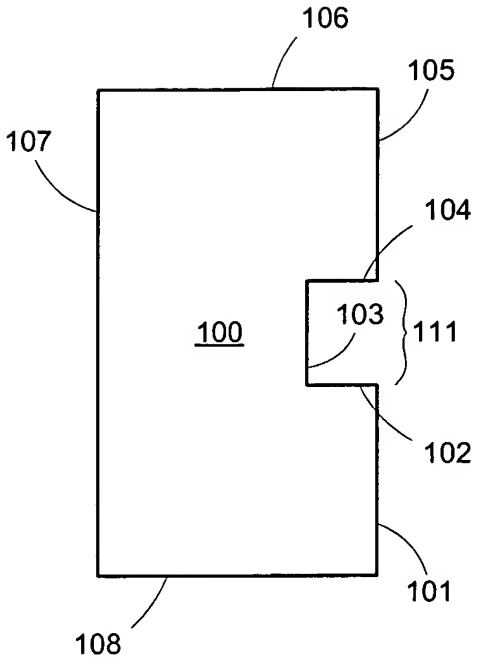


Fig. 1a
(PRIOR ART)

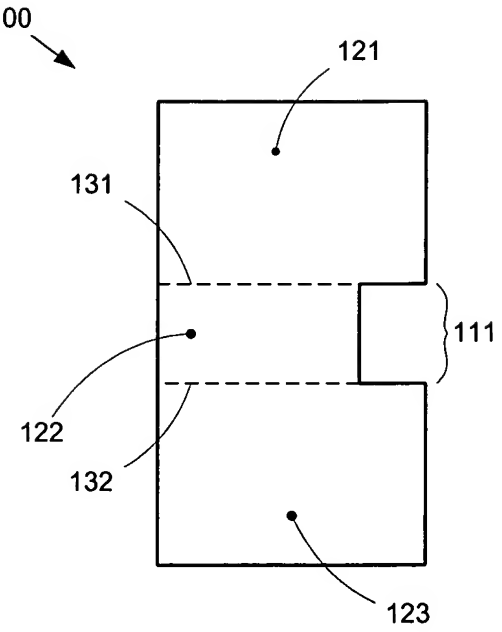


Fig. 1b
(PRIOR ART)

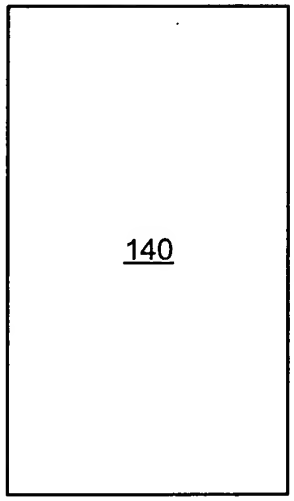


Fig. 1c
(PRIOR ART)

[0005] For example, Fig. 1a shows a simple polygon 100 made up of edges 101-108. Polygon 100 could represent a simple wire or interconnect in an IC layout. A notch 111 in the side of polygon 100 represents a common type of layout imperfection. If notch 111 is small, it may cause no significant electrical or optical problems. However, as shown in

Fig. 1b, during a fracturing operation notch 111 causes polygon 100 to be split into primitives 121, 122, and 123, along fracture lines 131 and 132. In contrast, Fig. 1c shows a polygon 140 that is substantially similar to polygon 100, but does not have the same notch-type imperfection. As a result, polygon 100 would fracture into a single primitive. Thus, the small imperfection in polygon 100 (i.e., notch 111 shown in Fig. 1b) results in a three-fold increase in data volume after a fracturing operation.

[0006] Unfortunately, due to the complexity of modern IC layouts, detecting and correcting this type of layout imperfection (a technique sometimes referred to as "layout beautification") can be difficult.

In accordance with one aspect of the invention, a layout beautification system uses a shape-based identification algorithm. As taught by Applicants in the Specification,

[0041] For example, Fig. 2b shows an example shape 220, which comprises edges 221, 222, and 223. Edges 211 and 213 are substantially similar in length. Edges 221 and 222 meet at a vertex 224 at an angle of 90 degrees, while edges 222 and 223 meet at a vertex 225 at an angle of 90 degrees. Edges 221 and 223 are parallel and side-by-side with one another, so that shape 220 has a C-shaped contour. Shape 220 could be used to detect notch-type defects anywhere in an IC layout, regardless of the layout configuration around each notch-type defect.

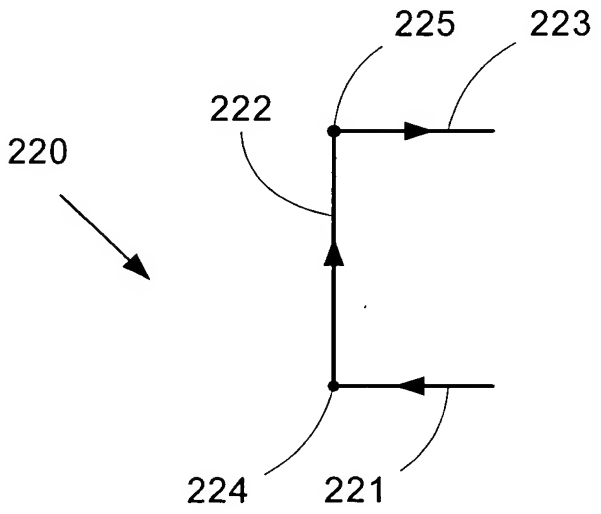


Fig. 2b

Another type of layout imperfection shown in Fig. 3b (see below), called necking, can occur because of the mismatch of shape widths that are overlapping. For example, the width of an interconnect polygon should match the width of a gate polygon for optimal electrical performance. This type of layout imperfection is extremely difficult to detect because the necking is not associated with any single polygon or even any single layer. Specification, paragraph [0044]. As further taught by Applicants in the Specification,

> [0045] … this type of layout imperfection can be readily detected and corrected by a shape-based layout beautification system. For example, Fig. 3b shows a shape 350 that includes contiguous edges 351-353, and contiguous edges 354-357. By associating edges 351-353 with the wire layer and edges 354-357 with the gate layer, shape 350 can be used to identify instances of the necking-type layout imperfection shown in Fig. 3a; i.e., edges 351-353 of shape 350 would correspond to edges 323-325, respectively, of interconnect polygon 320, while edges 354-357 of shape 350 would correspond to edges 311-314, respectively, of gate polygon 310. In addition, because shape 350 includes both the wire layer and gate layer information, a corrective action associated with shape 350 can accurately widen and align the connection formed by edges 323-325 of interconnect polygon with gate 310.

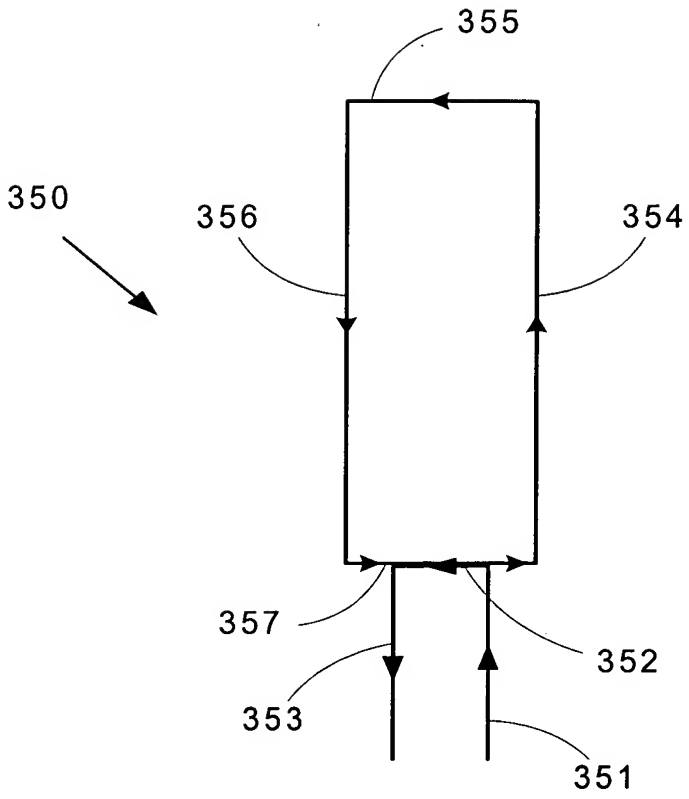


Fig. 3b

Another type of layout imperfection shown in Fig. 4b (see below), called a negative hammerhead, can also be difficult for standard tools to detect. As taught by Applicants in the paragraph [0046] of the Specification,

> Negative hammerheads are an OPC modification used to improve the optical performance of IC layout features (e.g., polygons or groupings of polygons) during lithography. However, OPC corrections are not necessary or even desirable in many situations. Where high optical precision is not required, OPC modifications (such as negative hammerheads) merely increase the data size and complexity of the IC layout, without providing any performance or manufacturability benefit. Unfortunately, because OPC tools often cannot distinguish between appropriate and inappropriate locations, OPC corrections must be applied in a blanket fashion.

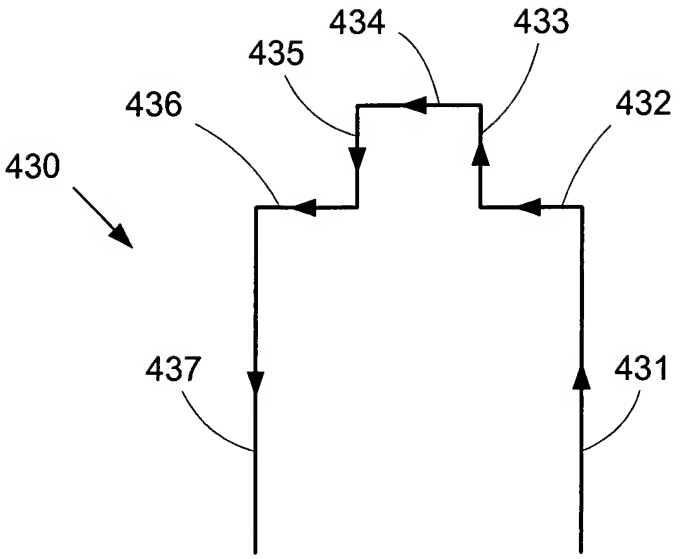


Fig. 4b

[0047] Once again, a shape-based system can enable detection of layout imperfections such as negative hammerheads. Fig. 4b shows a shape 430 comprising edges 431-437, which are arranged in a pattern similar to that of edges 411-417 of polygon 400 shown in Fig. 4a. By associating the appropriate properties (e.g., width between edges 431 and 437, length of edges 431 and 433, etc.) with the edges of shape 430, unwanted negative hammerheads in an IC layout can be detected.

Another type of layout imperfection shown in Fig. 5a (see below), called a stair-step, can also be corrected using layout beautification. Notably, the individual edges forming the stair-step are too nondescript to be readily detected by conventional edge-based systems, since such features cannot be easily distinguished from standard acceptable layout elements. Specification, paragraph [0049]. Furthermore, even if a single edge forming part of a stair-step pattern could be detected, correcting the associated step would change the characteristics of the neighboring steps, further complicating the detection efforts of conventional beautification systems. Specification, paragraph [0049]. As taught by Applicants in the paragraph

[0048] of the Specification in reference to Fig. 5a and 5c (shown below),

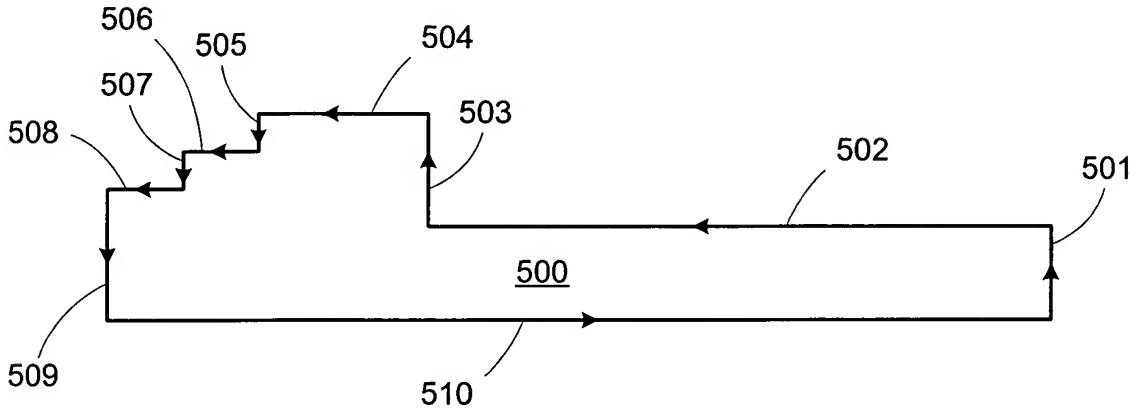


Fig. 5a

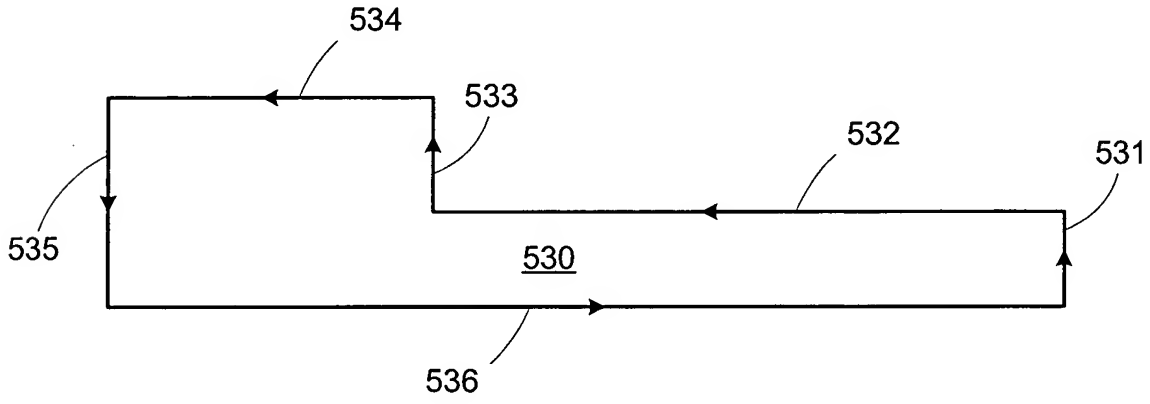


Fig. 5c

[0048] ... Polygon 500 comprises contiguous edges 501-510. The "stair-step" pattern formed by edges 505-508 can be produced by OPC operations, especially rule-based types of OPC. This type of stair-step pattern significantly increases layout data volume without a corresponding improvement in optical or electrical performance. Therefore, a polygon 530 shown in Fig. 5c, which comprises contiguous edges 531-536, provides a much more appropriate layout configuration. Polygon 530 replaces the stair-step pattern formed by edges 505-508 of polygon 500 with a single corner formed by edges 534 and 535. In this manner, polygon 530 reduces the edge-

count of polygon 500 by 4 edges (10 edges for polygon 500 versus only 6 edges for polygon 530).

[0051] Fig. 11a shows a polygon 1100 that includes another type of layout imperfection that would be difficult to detect and correct using conventional layout beautification methods. Polygon 1100 comprises contiguous edges 1101-1116. Edges 1109-1115 form a "stepped notch" 1119 in one side of polygon 1100. Stepped notch 1119 could, for example, be an OPC feature created to compensate for the angled profile of the bulge formed by edges 1103-1105. However, the stair-step configuration of stepped notch 1119 undesirably increases the data volume required by polygon 1100 without providing significant improvement in optical or electrical performance.

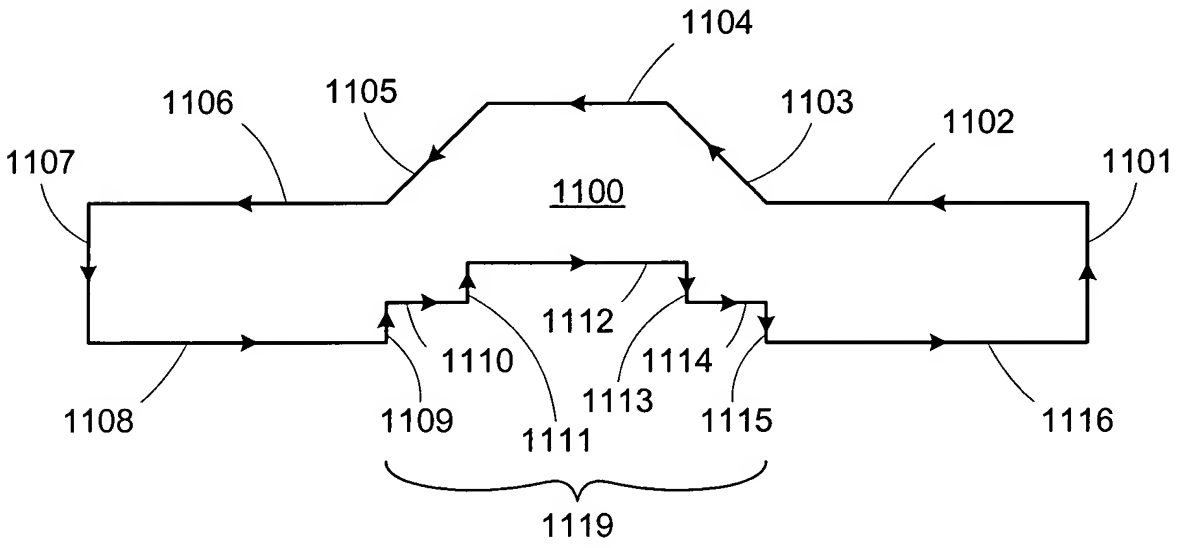


Fig. 11a

Applicants' system, apparatus, and method for providing layout beautification, which can correct the above-described layout imperfections, are reflected in at least the following claims.

Referring to Claim 11, an exemplary shape conforming to the recited edges is shown in Fig. 5a (e.g. edges 504, 505, 506, 507, and 508 could conform to the first, second, third, fourth, and fifth edges, respectively). Exemplary methods for performing a layout beautification operation are described in reference to Figs. 7 and 8.

Referring to Claim 33, the first and second set of instructions could refer to step 703 of Fig. 7 (matching and applying)(described in paragraphs [0072], [0073], [0074]) and the third set of instructions is described in paragraph [0056].

Referring to Claim 37, the first, second, and third set of instructions could refer to step 703 (matching and applying) and step 702 (loading) (Fig. 7) and are described in paragraphs [0072], [0073], [0074], and [0090].

Referring to Claim 38, the first and second set of instructions could refer to step 703 of Fig. 7 (matching and applying)(described in paragraphs [0072], [0073], [0074]) and the third set of instructions is described in paragraph [0056].

Referring to Claim 39, the first, second, and third set of instructions could refer to step 703 (matching and applying) and step 702 (loading) (Fig. 7) and are described in paragraphs [0072], [0073], [0074], and [0090].

Referring to Claim 40, the first and second set of instructions could refer to step 703 of Fig. 7 (matching and applying)(described in paragraphs [0072], [0073], [0074]). The third and fourth set of instructions could refer to step 703 after step 705 is answered in the affirmative.

Referring to Claim 41, completely executing the first and second set of instructions before the third and fourth set of instructions is shown in Fig. 7, for example.

Referring to Claim 42, concurrent execution of the first and second instructions and comparing the first shape before the second shape can refer to steps 701, 703, and 705 of Fig. 7 (described in paragraphs [0072], [0073], [0074]).

Referring to Claim 55, the step of applying a first action responsive to a match can refer to step 703 (Fig. 7) and exemplary layout imperfections are shown in Figs. 2a, 3b, 4b, 5a, 11a, and 12a.

Referring to Claim 56, adjusting the first type of layout imperfection by a fixed amount is described in paragraph [0060].

Referring to Claim 57, the first type of layout imperfection covering a plurality of actual layout imperfections, each of the plurality of actual layout imperfections having a different set of actual properties, wherein the first action comprises making an adjustment according to the set of actual properties for each of the plurality of actual layout imperfections is described in paragraph [0061].

Referring to Claim 58, replacing a layout imperfection with another shape is described in paragraph [0048].

Referring to Claim 64, an exemplary shape conforming to the recited configuration is shown by edges 411-417 (first to seventh edges, respectively) of polygon 400 in Fig. 4a.

Referring to Claim 65, defining the shapes, defining the actions, and applying the actions is described in paragraphs [0029-0039], [0010, 0012, 0090], and [0045, 0046, 0047, 0048, 0052], respectively. Exemplary layout imperfections are shown in Figs. 2a, 3b, 4b, 5a, 11a, and 12a.

Referring to Claim 67, determining a sequence based on a ranking of imperfection criticality is described in paragraph [0081].

Referring to Claim 72, an exemplary system for performing layout beautification is shown and described in reference to Fig. 9.

Referring to Claim 73, reassembling layout primitives into polygons is described in paragraph [0079].

Referring to Claim 79, an exemplary system for performing layout beautification is shown and described in reference to Fig. 9.

Referring to Claim 85, the first and second set of instructions could refer to step 703 of Fig. 7 (matching and applying) (described in paragraphs [0072], [0073], [0074]).

Referring to Claim 89, the means for identifying and the means for replacing can perform step 703 of Fig. 7, as described in paragraphs [0072], [0073], [0074], and [0052].

Referring to Claim 91, identifying and modifying could refer to step 703 of Fig. 7 (matching and applying) (described in paragraphs [0072], [0073], [0074]). The first, second, and third operations are described in paragraphs [0060], [0061], [0062], and [0063].

Referring to Claim 96, identifying and applying could refer to step 703 of Fig. 7 (described in paragraphs [0072], [0073], [0074]). The absolute, adaptive, and replacement operations are described in paragraphs [0060], [0061], [0062], and [0063].

Referring to Claim 99, the replacement correction is described in paragraph [0052].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following issues are presented to the Board of Appeals for decision:

(A) Whether Claims 11, 33, 37-43, and 55-99 are patentable under 35 U.S.C. 102(e) over U.S. Patent 6,523,162 (Agrawal).

(B) Whether minor objections prevent a review on the merits.

VIII. ARGUMENTS

A. Claims 11, 33, 37-43, and 55-99 are patentable under 35 U.S.C. 102(e) over U.S. Patent 6,523,162 (Agrawal)

1. Agrawal Overview

Agrawal teaches applying layout processing to an IC layout using a shape-based identification system. Col. 3, lines 19-22. A shape can be defined as a set of associated edges. Col. 3, lines 22-23. A catalog of shapes can be defined and layout processing actions can be formulated based on the properties of the various shapes. Col. 3, lines 25-27. A library of layout processing actions associated with the shapes can be rule-based, model-based, or can provide any other response a user would like implemented (i.e. "layout processing" can include OPC, phase shift mask (PSM), design rule checking (DRC), "fracturing" of layout features for e-beam mask making machines etc.). Col. 3, line 63 to col. 4, line 1.

Figs. 9a-9c of Agrawal provide an example to illustrate two types of conflicts (i.e. shape and action conflicts). Col. 10, lines 48-61. Action A (Fig. 9a) applies a serif to a corner whereas action B (Fig. 9b) narrows and lengthens a finger structure. Fig. 9c illustrates a shape conflict that can result in an action conflict (i.e. the incompatibility of actions A and B). Notably, actions A and B are OPC actions, not actions associated with layout beautification. See, col. 11, lines 1-10.

2. Applicants' limitations recited in Claims 11, 33, 37-43, and 55-99 are not taught by Agrawal.

Agrawal fails to disclose or suggest layout beautification or a layout imperfection as recited in the claims. Agrawal teaches that a shape-based identification system can be advantageously used for applying layout processing to an IC layout. Col. 3, lines 19-22. As taught by Agrawal, layout processing can include optical proximity correction (OPC),

design rule checking (DRC), phase shift mask (PSM), fracturing, etc. col. 3, line 66 to col. 4, line 1.

Applicants have advantageously recognized the problem presented by layout imperfections, which are electrically correct and yet adversely affect layout printability or device performance. Specification, paragraph [0004]. Moreover, layout imperfections can significantly increase data volume for a particular IC layout, thereby undesirably increasing layout processing (e.g. OPC, DRC, etc.) and mask production times. Specification, paragraph [0004].

Thus, layout beautification, which corrects such layout imperfections, is distinct from other types of layout processing (e.g. OPC, DRC, and fracturing). Notably, Agrawal fails to recognize the problem of layout imperfections and the benefits to applying shape identification to layout beautification.

Claim 11 recites:

> A method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons, the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout,
>
> the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection,
>
> the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises:
>
> a third edge, the third edge being contiguous with and substantially perpendicular to the second edge;
>
> a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge; and
>
> a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein none of the first edge, the second edge,

the third edge, the fourth edge, and the fifth edge are substantially side-by-side with each other.

The passages of Agrawal cited in the Final Office Action with respect to Claim 11 (i.e. col. 14, lines 16-19; col. 5, lines 51-52; col. 8, lines 45-48; col. 14, line 31; col. 14, lines 24-30; col. 14, lines 20-23; col. 6, lines 35-37; col. 6, lines 44-51; and col. 17, lines 10-21) fail to disclose or suggest the recited layout beautification and layout imperfection.

Moreover, the Final Office Action cites multiple figures in Agrawal for each of the recited edges in Claim 11. Specifically, Figs. 4a, 4b, 4c, 5a, 5b, 5c, 5d, 6a, 6b, 6c, 6d, 6e, 7a, 7b, 7c are cited as teaching the recited first, second, third, fourth, and fifth edges. Applicants submit that such picking and choosing from various shapes is inappropriate.

An exemplary shape conforming to the recited edges is shown in Fig. 5a. In Fig. 5a, the "stair-step" pattern formed by edges 504-508 can be produced by OPC operations, especially rule-based types of OPC. Specification, paragraph [0048]. This type of stair-step pattern significantly increases layout data volume without a corresponding improvement in optical or electrical performance. Specification, paragraph [0048]. Once this shape is correctly identified, in accordance with Applicants' invention, polygon 500 of Fig. 5a can be replaced with polygon 530 of Fig. 5c, thereby reducing the edge count. Agrawal fails to teach the first shape having the recited first, second, third, fourth, and fifth edges.

Because Agrawal fails to disclose or suggest layout beautification, layout imperfection, and the recited edge configuration, Applicant submits that Claim 11 is patentable over Agrawal.

Claim 33 recites:

A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property;

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for defining the first shape according to a set of user inputs.

The passages of Agrawal cited in the Final Office Action with respect to Claim 33 (i.e. col. 19, lines 25-26; col. 20, lines 1-7, 20-25; and abstract) fail to disclose or suggest the recited layout beautification. Therefore, Applicants submit that Claim 33 is patentable over Agrawal.

Claim 37 recites:

A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property;

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for loading the first shape from across a network.

The passages of Agrawal cited in the Final Office Action with respect to Claim 37 (i.e. col. 13, lines 51-53; col. 19, lines 25-26; col. 20, lines 1-7, 16-24; and abstract) fail to

disclose or suggest the recited layout beautification action. Therefore, Applicants submit that Claim 37 is patentable over Agrawal.

Claim 38 recites:

> A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:
>
> a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property;
>
> a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and
>
> a third set of instructions for defining the first layout beautification action according to a set of user inputs.

The passages of Agrawal cited in the Final Office Action with respect to Claim 38 (i.e. col. 19, lines 25-26; col. 20, lines 1-7, 16-22; and abstract) fail to disclose or suggest the recited layout beautification action. Therefore, Applicants submit that Claim 38 is patentable over Agrawal.

Claim 39 recites:

> A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:
>
> a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and
>
> a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for loading the first action from across a network.

The passages of Agrawal cited in the Final Office Action with respect to Claim 39 (i.e. col. 13, lines 51-53; col. 19, lines 25-26; col. 20, lines 1-7, 16-24; and abstract) fail to disclose or suggest the recited layout beautification action. Therefore, Applicants submit that Claim 39 is patentable over Agrawal.

Claim 40 recites:

A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for comparing a second shape to the plurality of features in each of the plurality of polygons to identify a second set of matching layout features, the second shape comprising at least a third edge and a fourth edge related according to a second property; and

a fourth set of instructions for performing a second layout beautification action on the second set of matching layout features.

The passages of Agrawal cited in the Final Office Action with respect to Claim 40 (i.e. col. 19, lines 13-26; col. 20, lines 1-7, 16-19; and abstract) fail to disclose or suggest the recited layout beautification actions. Therefore, Applicants submit that Claim 40 is patentable over Agrawal.

Claims 41-43 depend from Claim 40 and therefore are patentable over Agrawal for at least the reasons presented for Claim 40.

Moreover, Claim 41 recites "wherein the first set of instructions and the second set of instructions are completely executed before the third set of instructions and the fourth set of instructions." The Final Office Action cites col. 20, lines 16-19 as teaching this limitation. Applicants traverse this characterization. Col. 20, lines 16-19 teach nothing regarding the execution order of the recited sets of instructions. Therefore, Applicants submit that Claim 41 is further patentable over Agrawal.

Moreover, Claim 42 recites "wherein the first set of instructions and the second set of instructions are executed concurrently, and wherein comparing the first shape to a selected one of the plurality of features in each of the plurality of polygons is performed before comparing the second shape to the selected one of the plurality of features in each of the plurality of polygons." The Final Office Action cites col. 3, lines 14-16 and col. 19, lines 22-24 as teaching this limitation. Applicants traverse this characterization. Col. 3, lines 14-16 and col. 19, lines 22-24 teach nothing regarding the execution order of the recited sets of instructions. Therefore, Applicants submit that Claim 42 is further patentable over Agrawal.

Claim 55 recites:

> A method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons, the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout, the first shape comprising at least a first edge and a second edge related according to a defined property, the first

shape being configured to match a first type of layout imperfection.

The Final Office Action cites col. 5, lines 51-52; col. 8, lines 45-48; and col. 14, lines 16-31 as teaching these limitations. Applicants traverse this characterization. These passages fail to disclose or suggest the recited layout beautification and layout imperfection. Therefore, Applicants submit that Claim 55 is patentable over Agrawal.

Claims 56-64 depend from Claim 55 and therefore are patentable over Agrawal for at least the reasons presented for Claim 55.

Moreover, Claim 56 recites "wherein the first action comprises adjusting the first type of layout imperfection by a fixed amount." The Final Office Action cites col. 10, lines 64-67 and Fig. 9b as teaching this limitation. Applicants traverse this characterization. Action B of narrowing and lengthening a finger structure fails to teach adjusting a first type of layout imperfection. Therefore, Applicants submit that Claim 56 is further patentable over Agrawal.

Moreover, Claim 57 recites "wherein the first type of layout imperfection covers a plurality of actual layout imperfections, each of the plurality of actual layout imperfections having a different set of actual properties, wherein the first action comprises making an adjustment according to the set of actual properties for each of the plurality of actual layout imperfections." The Final Office Action cites col. 3, lines 24-26 and col. 6, lines 14-18 as teaching these limitations. Applicants traverse this characterization. These passages fail to disclose or suggest layout imperfections, much less making an adjustment according to actual properties for each layout imperfection. Therefore,

Applicants submit that Claim 57 is further patentable over Agrawal.

Moreover, Claim 58 recites "wherein the first action comprises replacing the first type of layout imperfection with a second shape." The Final Office Action cites col. 8, lines 37-39 and col. 10, lines 34-36 as teaching this limitation. Applicants traverse this characterization. These passages fail to disclose or suggest a first type of layout imperfection, much less replacing the first type of layout imperfection with a second shape. Therefore, Applicants submit that Claim 58 is further patentable over Agrawal.

Moreover, Claim 64 recites:

> The method of Claim 55, the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises:
>
> a third edge, the third edge being contiguous with and substantially perpendicular to the second edge, wherein the third edge is not substantially side-by-side with the first edge;
>
> a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge, wherein the fourth edge is not substantially side-by-side with the second edge;
>
> a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein the fifth edge is substantially parallel to and side-by-side with the third edge;
>
> a sixth edge, the sixth edge being contiguous with and substantially perpendicular to the fifth edge, wherein the sixth edge is not substantially side-by-side with the fourth edge; and
>
> a seventh edge, the seventh edge being contiguous with and substantially perpendicular to the sixth edge, the seventh edge being substantially parallel to and side-by-side with the first edge.

The Final Office Action cites the edges of shape 660 in Fig. 6d as teaching this configuration. Applicants traverse this characterization. Shape 660 fails to teach multiple edges of

the recited configuration. An exemplary shape conforming to the recited configuration is shown by edges 411-417 of polygon 400 in Fig. 4a. As taught by Applicants in paragraph [0046]:

> The inverted serif created by edges 412 and 413, and the inverted serif created by edges 415 and 416 form a pattern sometimes referred to as a "negative hammerhead." Negative hammerheads are an OPC modification used to improve the optical performance of IC layout features (e.g., polygons or groupings of polygons) during lithography. However, OPC corrections are not necessary or even desirable in many situations. Where high optical precision is not required, OPC modifications (such as negative hammerheads) merely increase the data size and complexity of the IC layout, without providing any performance or manufacturability benefit. Unfortunately, because OPC tools often cannot distinguish between appropriate and inappropriate locations, OPC corrections must be applied in a blanket fashion

Agrawal fails to disclose or suggest this recited configuration of edges. Therefore, Applicants submit that Claim 64 is further patentable over Agrawal.

Claim 65 recites:

> A method for correcting a plurality of layout imperfections in an integrated circuit (IC) layout, the method comprising:
>
> defining a plurality of shapes, each of the plurality of shapes comprising at least a first edge and a second edge related according to at least one of a plurality of defined properties, each of the plurality of shapes matching at least one of the plurality of layout imperfections;
>
> defining a plurality of actions to correct the plurality of layout imperfections, each of the plurality of actions being associated with at least one of the plurality of shapes; and
>
> applying the plurality of actions to the IC layout responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements within the IC layout.

The Final Office Action cites col. 5, lines 51-52, col. 8, lines 45-58, col. 14, lines 16-23, and the abstract as teaching these limitations. Applicants traverse this characterization. These passages fail to disclose or suggest layout imperfections. Therefore, Applicants submit that Claim 65 is patentable over Agrawal.

Claims 66-71 depend from Claim 65 and therefore are patentable over Agrawal for at least the reasons presented above for Claim 65.

Moreover, Claim 67 recites "the specified sequence being determined according to a predefined ranking of layout imperfection criticality." The Final Office Action cites col. 4, lines 22-27 as teaching this limitation. Applicants traverse this characterization. This passage refers to shape complexity, not layout imperfection criticality. Therefore, Applicants submit that Claim 67 is further patentable over Agrawal.

Claim 72 recites:

> A system for performing layout beautification on an integrated circuit (IC) layout data file, the system comprising:
>
> an input data manager for loading the IC layout data file into the system;
>
> a layout beautification engine for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and
>
> an output data manager for generating an output data file.

The Final Office Action cites col. 12, lines 17-22, 49-60, and Fig. 10a as teaching these limitations. Applicants traverse this characterization. These passages and figure fail to

disclose or suggest a layout beautification engine. Therefore, Applicants submit that Claim 72 is patentable over Agrawal.

Claims 73-78 depend from Claim 72 and therefore are patentable over Agrawal for at least the reasons presented above for Claim 72.

Moreover, Claim 73 recites, "wherein the IC layout data file comprises a fractured data file, and wherein loading the IC layout data file into the system comprises reassembling a plurality of layout primitives into a plurality of polygons." The Final Office Action cites col. 18, lines 56-59 as teaching these limitations. Applicants traverse this characterization. This passage relates to an action comprising a definition of a fracturing operation, not the recited fractured data file (which would require reassembly when loading). Therefore, Applicants submit that Claim 73 is further patentable over Agrawal.

Claim 79 recites:

> A system for performing layout beautification on an integrated circuit (IC) layout data file, the system comprising:
>
> means for loading the IC layout data file into the system;
>
> means for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and
>
> means for generating an output data file.

The Final Office Action cites col. 12, lines 17-22, 49-60, and Fig. 10a as teaching these limitations. Applicants traverse this characterization. These passages and figure fail to disclose or suggest performing layout beautification. Applicants note that the IC layout data file is recited first in the preamble and then recited subsequently in the body of the

claim. In Claim 70, the preamble recites limitations of the claim and is 'necessary to give life, meaning, and vitality' to the claim. Therefore, Applicant submits that the preamble recitation of performing layout beautification should be construed as if in the balance of the claim. Piney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305 (Fed. Cir. 1999). Because Agrawal fails to disclose or suggest a system for performing layout beautification, Applicants submit that Claim 79 is patentable over Agrawal.

Claims 80-84 depend from Claim 79 and therefore are patentable over Agrawal for at least the reasons presented above for Claim 79.

Claim 85 recites:

> A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:
>
> a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and
>
> a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features.

The Final Office Action cites col. 19, lines 25-26 and col. 20, lines 1-7, 20-25 as teaching these limitations. Applicants traverse this characterization. These passages fail to disclose or suggest performing a layout beautification action. Because Agrawal fail to disclose or suggest a software program for performing layout beautification as well as the second set of instructions for performing a first layout beautification action, Applicants submit that Claim 85 is patentable over Agrawal.

Claims 86-88 depend from Claim 85 and therefore are patentable over Agrawal for at least the reasons presented above for Claim 85.

Claim 89 recites:

> An apparatus for reducing output data size in an input layout by beautifying the input layout, the apparatus comprising:
>
> means for identifying a shape pattern in the input layout, wherein the shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and
>
> means for replacing the identified shape pattern with an alternative configuration, the alternative configuration reducing data volume.

The Final Office Action cites col. 5, lines 59-61, col. 8, lines 18-21, col. 14, lines 20-24, the abstract, and Figs. 3a, 7d, and 11 as teaching these limitations. Applicants traverse this characterization. These passages and figures fail to disclose or suggest beautifying the input layout as well as reducing data volume using an alternative configuration. Applicants note that the input layout is recited first in the preamble and then recited subsequently in the body of the claim. In Claim 89, the preamble recites limitations of the claim and is 'necessary to give life, meaning, and vitality' to the claim. Therefore, Applicant submits that the preamble recitation of beautifying the input layout should be construed as if in the balance of the claim. Piney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305 (Fed. Cir. 1999). Because Agrawal fails to disclose or suggest an apparatus for reducing output data size in an input layout by beautifying the input layout, Applicants submit that Claim 89 is patentable over Agrawal.

Claim 90 depends from Claim 89 and therefore is patentable over Agrawal for at least the reasons presented above for Claim 89.

Claim 91 recites:

> A method of providing corrective actions to a layout based on shape analysis, the method comprising:
> identifying shape patterns on the layout, wherein each shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and
> modifying the layout according to corrective actions associated with the identified shape patterns, thereby removing at least one layout imperfection, wherein the corrective actions include at least one of:
> performing a first operation using a fixed value associated with an existing layout parameter of an identified shape pattern;
> performing a second operation that is a function of an existing layout parameter of an identified shape pattern; and
> performing a third operation that replaces an identified shape pattern.

The Final Office Action cites col. 4, lines 49-50, 45-48, col. 5, lines 51-52, col. 8, lines 45-48, col. 14, lines 16-23, as teaching these limitations. Applicants traverse this characterization. These passages fail to disclose or suggest removing at least one layout imperfection. Therefore, Applicants submit that Claim 91 is patentable over Agrawal.

Claims 92-95 depend from Claim 91 and therefore are patentable over Agrawal for at least the reasons presented above for Claim 91.

Claim 96 recites:

> A shape-based beautification method in a layout, the method comprising:
> identifying a shape pattern on the layout; and
> applying at least one of an absolute correction, an adaptive correction, and a replacement correction to the identified shape pattern, thereby removing at least one layout imperfection and reducing fracturing data volume in the layout.

The Final Office Action cites col. 4, lines 45-50, col. 5, lines 51-52, col. 8, lines 45-48, col. 12, lines 31-37, and col. 14, lines 16-23, as teaching these limitations. Applicants traverse this characterization. These passages fail to disclose or suggest a shape-based beautification method, removing at least one layout imperfection, and reducing fracturing data volume in the layout. Applicants note that the layout is recited first in the preamble and then recited subsequently in the body of the claim. In Claim 96, the preamble recites limitations of the claim and is 'necessary to give life, meaning, and vitality' to the claim. Therefore, Applicant submits that the preamble recitation of a shape-based beautification method should be construed as if in the balance of the claim. Piney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305 (Fed. Cir. 1999). Because Agrawal fails to disclose or suggest a shape-based beautification method, removing at least one layout imperfection, and reducing fracturing data volume in the layout, Applicants submit that Claim 96 is patentable over Agrawal.

Claims 97-99 depend from Claim 96 and therefore are patentable over Agrawal for at least the reasons presented above for Claim 96.

Moreover, Claim 99 recites, "wherein the replacement correction replaces the identified shape pattern with a simplified shape pattern." The Final Office Action cites col. 4, lines 45-48 as teaching this limitation. Applicants traverse this characterization. The "filler shapes" taught in this passage are used for shape identification/matching, not as replacement shapes. These filler shapes are discussed in further detail in col. 14, lines 6-9. Because Agrawal fails to disclose or suggest the recited simplified shape pattern,

Applicants submit that Claim 99 is further patentable over Agrawal.

B. Objections to Specification and Claim 87 should not prohibit review on the merits.

The Final Office Action objects to the Specification based on a typographical error (paragraph [0076]: "beatification" needs to be replaced with "beautification". Applicants submit that such correction can be easily addressed after resolution of this appeal.

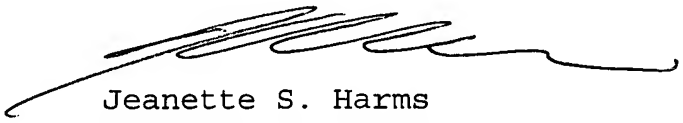
The Final Office Action also objects to the use of the word "can" in Claim 87 and requires its deletion. Applicants submit that such deletion can also be easily addressed after resolution of this appeal.

Therefore, Applicants submit that these objections should not prohibit a review of this case on the merits.

C. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejections of Claims 11, 33, 37-43, and 55-99 are erroneous, and reversal of these rejections is respectfully requested.

Respectfully submitted,



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6/16/2005 Rebecca A Baumann
Date Signature: Rebecca A. Baumann

VIII. CLAIMS APPENDIX

1-10 (Cancelled)

11. (Previously Presented) A method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons, the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout,

the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection,

the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises:

a third edge, the third edge being contiguous with and substantially perpendicular to the second edge;

a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge; and

a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein none of the first edge, the second edge, the third edge, the fourth edge, and the fifth edge are substantially side-by-side with each other.

12-32 (Cancelled)

33. (Previously Presented) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of

polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for defining the first shape according to a set of user inputs.

34-36. (Cancelled)

37. (Previously Presented) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for loading the first shape from across a network.

38. (Previously Presented) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for defining the first layout beautification action according to a set of user inputs.

39. (Previously Presented) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for loading the first action from across a network.

40. (Previously Presented) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for comparing a second shape to the plurality of features in each of the plurality of polygons to identify a second set of matching layout features, the second shape comprising at least a third edge and a fourth edge related according to a second property; and

a fourth set of instructions for performing a second layout beautification action on the second set of matching layout features.

41. (Previously Presented) The software program of Claim 40, wherein the first set of instructions and the second set of

instructions are completely executed before the third set of instructions and the fourth set of instructions.

42. (Previously Presented) The software program of Claim 40, wherein the first set of instructions and the second set of instructions are executed concurrently, and wherein comparing the first shape to a selected one of the plurality of features in each of the plurality of polygons is performed before comparing the second shape to the selected one of the plurality of features in each of the plurality of polygons.

43. (Previously Presented) The software program of Claim 40, wherein first action and the second action are incorporated in a lookup table.

44-54. (Cancelled)

55. (Previously Presented) A method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons, the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout, the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection.

56. (Previously Presented) The method of Claim 55, wherein the first action comprises adjusting the first type of layout imperfection by a fixed amount.

57. (Previously Presented) The method of Claim 55, wherein the first type of layout imperfection covers a plurality of actual layout imperfections, each of the plurality of actual layout imperfections having a different set of actual properties, wherein the first action comprises making an adjustment according to the set of actual properties for each of the plurality of actual layout imperfections.

58. (Previously Presented) The method of Claim 55, wherein the first action comprises replacing the first type of layout imperfection with a second shape.

59. (Previously Presented) The method of Claim 55, wherein the first edge and the second edge are not contiguous.

60. (Previously Presented) The method of Claim 59, wherein the IC layout comprises a first layer and a second layer, the first edge being associated with the first layer, and the second edge being associated with the second layer.

61. (Previously Presented) The method of Claim 60, wherein the first layer comprises a gate layer, and wherein the second layer comprises a wire layer.

62. (Previously Presented) The method of Claim 55, wherein the defined property specifies a plurality of alternative relationships between the first edge and the second edge.

63. (Previously Presented) The method of Claim 55, the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises a third edge, the third edge being contiguous

with and substantially perpendicular to the second edge, the third edge being substantially parallel to and side-by-side with the first edge.

64. (Previously Presented) The method of Claim 55, the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises:

a third edge, the third edge being contiguous with and substantially perpendicular to the second edge, wherein the third edge is not substantially side-by-side with the first edge;

a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge, wherein the fourth edge is not substantially side-by-side with the second edge;

a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein the fifth edge is substantially parallel to and side-by-side with the third edge;

a sixth edge, the sixth edge being contiguous with and substantially perpendicular to the fifth edge, wherein the sixth edge is not substantially side-by-side with the fourth edge; and

a seventh edge, the seventh edge being contiguous with and substantially perpendicular to the sixth edge, the seventh edge being substantially parallel to and side-by-side with the first edge.

65. (Previously Presented) A method for correcting a plurality of layout imperfections in an integrated circuit (IC) layout, the method comprising:

defining a plurality of shapes, each of the plurality of shapes comprising at least a first edge and a second edge related according to at least one of a plurality of defined properties, each of the plurality of shapes matching at least one of the plurality of layout imperfections;

defining a plurality of actions to correct the plurality of layout imperfections, each of the plurality of actions being associated with at least one of the plurality of shapes; and

applying the plurality of actions to the IC layout responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements within the IC layout.

66. (Previously Presented) The method of Claim 65, the plurality of actions having a specified sequence, wherein any element within the IC layout to which one of the plurality of actions is applied is excluded from further applications of the plurality of actions.

67. (Previously Presented) The method of Claim 66, the specified sequence being determined according to a predefined ranking of layout imperfection criticality.

68. (Previously Presented) The method of Claim 65, the IC layout comprising a plurality of polygons, each of the plurality of polygons comprising a plurality of elements, wherein applying the plurality of actions to the IC layout comprises:

applying the plurality of actions to the plurality of elements included in a first polygon in the plurality of polygons in a specified sequence; and

restarting the specified sequence when one of the plurality of actions is applied to one of the elements of the IC layout included in the first polygon.

69. (Previously Presented) The method of Claim 65, wherein applying the plurality of actions to the IC layout comprises:

applying a first action to the IC layout responsive to the at least one of the plurality of shapes associated with the first action matching elements in the IC layout; and

applying a second action to the IC layout responsive to the at least one of the plurality of shapes associated with the second action matching elements in the IC layout.

70. (Previously Presented) The method of Claim 65, the IC layout comprising a plurality of polygons, wherein applying the plurality of actions to the IC layout comprises:

applying each of the plurality of actions to a first polygon in the plurality of polygons responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements in the first polygon; and

applying each of the plurality of actions to a second polygon in the plurality of polygons responsive to the at least one of the plurality of shapes associated with the plurality of actions matching elements in the second polygon.

71. (Previously Presented) The method of Claim 70, further comprising initializing a lookup table, the lookup table incorporating the plurality of actions.

72. (Previously Presented) A system for performing layout beautification on an integrated circuit (IC) layout data file, the system comprising:

an input data manager for loading the IC layout data file into the system;

a layout beautification engine for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and

an output data manager for generating an output data file.

73. (Previously Presented) The system of Claim 72, wherein the IC layout data file comprises a fractured data file, and wherein loading the IC layout data file into the system comprises reassembling a plurality of layout primitives into a plurality of polygons.

74. (Previously Presented) The system of Claim 72, the IC layout data file having a first data file format, wherein loading the IC layout data file into the system comprises converting the first data file format into a second data file format, the layout beautification engine being configured to operate on the second data file format.

75. (Previously Presented) The system of Claim 74, wherein generating the output data file comprises converting the second data file format into a third data file format.

76. (Previously Presented) The system of Claim 72, wherein the layout beautification engine comprises a lookup table incorporating the plurality of corrective actions.

77. (Previously Presented) The system of Claim 72 further comprising a network connection to a remote storage location, wherein the remote storage location stores at least one of the IC layout data file and the plurality of corrective actions.

78. (Previously Presented) The system of Claim 77, wherein the plurality of corrective actions are incorporated in a lookup table.

79. (Previously Presented) A system for performing layout beautification on an integrated circuit (IC) layout data file, the system comprising:

means for loading the IC layout data file into the system;

means for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and

means for generating an output data file.

80. (Previously Presented) The system of Claim 79, the IC layout data file comprising a plurality of layers, wherein the means for loading the IC layout data file into the system

comprises means for selecting at least one of the plurality of layers.

81. (Previously Presented) The system of Claim 79, the IC layout data file having a first data file format, wherein the means for loading the IC layout data file into the system comprises means for converting the first data file format into a second data file format, wherein the means for applying a plurality of corrective actions to the IC layout data file operates on the second data file format.

82. (Previously Presented) The system of Claim 81, wherein the means for generating the output data file comprises means for converting the second data file format into a third data file format.

83. (Previously Presented) The system of Claim 79, wherein the means for generating the output data file further comprises means for allowing a user to select the third data file format from a plurality of data file formats.

84. (Previously Presented) The system of Claim 79 further comprising means for accessing a remote storage location, wherein the remote storage location stores at least one of the IC layout data file and the plurality of corrective actions.

85. (Previously Presented) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features.

86. (Previously Presented) The software program of Claim 85, wherein the first layout beautification action comprises modifying each of the first set of matching features by a fixed amount.

87. (Previously Presented) The software program of Claim 85, wherein each of the first set of matching features can comprise a different characteristic, and wherein the first layout beautification action comprises performing a modification on each of the first set of matching features, the modification being based on the different characteristic of each of the first set of matching features.

88. (Previously Presented) The software program of Claim 85, wherein the first layout beautification action comprises replacing each of the first set of matching features with a second shape.

89. (Previously Presented) An apparatus for reducing output data size in an input layout by beautifying the input layout, the apparatus comprising:

means for identifying a shape pattern in the input layout, wherein the shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and

means for replacing the identified shape pattern with an alternative configuration, the alternative configuration reducing data volume.

90. (Previously Presented) The apparatus of Claim 89, wherein the alternative configuration provides one of an absolute correction, an adaptive correction, and a replacement correction.

91. (Previously Presented) A method of providing corrective actions to a layout based on shape analysis, the method comprising:

identifying shape patterns on the layout, wherein each shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and

modifying the layout according to corrective actions associated with the identified shape patterns, thereby removing at least one layout imperfection, wherein the corrective actions include at least one of:

performing a first operation using a fixed value associated with an existing layout parameter of an identified shape pattern;

performing a second operation that is a function of an existing layout parameter of an identified shape pattern; and

performing a third operation that replaces an identified shape pattern.

92. (Previously Presented) The method of Claim 91, wherein performing the first operation includes matching a dimensional specification of a design rule and the existing layout parameter.

93. (Previously Presented) The method of Claim 91, wherein performing the first operation includes fixed biasing.

94. (Previously Presented) The method of Claim 91, wherein performing the second operation includes providing a corrective action proportional to the existing layout parameter.

95. (Previously Presented) The method of Claim 91, wherein performing the second operation includes at least one of proportional biasing and negative biasing.

96. (Previously Presented) A shape-based beautification method in a layout, the method comprising:

identifying a shape pattern on the layout; and

applying at least one of an absolute correction, an adaptive correction, and a replacement correction to the identified shape pattern, thereby removing at least one layout imperfection and reducing fracturing data volume in the layout.

97. (Previously Presented) The method of Claim 96, wherein the absolute correction includes matching a dimensional specification of a design rule and an existing layout parameter of the identified shape pattern.

98. (Previously Presented) The method of Claim 96, wherein the adaptive correction includes providing a corrective action proportional to the existing layout parameter.

99. (Previously Presented) The method of Claim 96, wherein the replacement correction replaces the identified shape pattern with a simplified shape pattern.

IX. EVIDENCE APPENDIX

None

X. RELATED PROCEEDINGS APPENDIX

None